# Low-voltage CCII based all-pass/notch filter

Susheel Sharma<sup>1</sup>, S S Rajput<sup>2</sup>, K Pal<sup>3</sup>, L K Mangotra<sup>1</sup> & S S Jamuar<sup>4</sup>

<sup>1</sup>Department of Physics & Electronics, University of Jammu, Jammu 180 006
<sup>2</sup>National Physical Laboratory, Dr K S Krishnan Marg, New Delhi 110 012
<sup>3</sup>Department of Earthquake Engineering, Indian Institute of Technology, Roorkee
<sup>4</sup>Department of Electrical & Electronic Engineering, University Putra Malaysia, Malaysia

Received 1 September 2005; revised 13 February 2006; accepted 8 September 2006

A second order low-voltage ( $\pm$  0.75 V) second-generation current conveyor (CCII) based filter circuit has been presented which can realize dual filter functions (all-pass/notch) depending on the resistance ratio. The gain of the filter is independently controlled by a resistance. The circuit employs almost all grounded components (except one resistor), thus enables its implementation with standard CMOS technologies. Theoretical results have been verified by PSpice simulations using 0.5 µm technology parameters.

Keywords: Low voltage circuit, Floating-gate MOSFET, Current conveyor, Active filter

IPC Code: H03H

## **1** Introduction

Filters are important components of modern communication and instrumentation systems and need to be operated from low supply voltages for mobile applications. Operating circuits with low supply voltage is a common technique to yield low power dissipation, which is essential for enhancing the battery life<sup>1-3</sup>. A low voltage CCII can be designed by using low voltage circuit design techniques. The use of Floating gate MOSFET (FGMOS) is one such technique where it is possible to reduce threshold voltage without device scaling<sup>4-6</sup>. A CCII has been regarded as the most versatile circuit building block used extensively in filtering and other applications, exhibiting its performance superiority over the conventional op amps<sup>7-19</sup>.

Active filters with high input impedance have great significance as they can be easily cascaded to realize higher order filters without any loading effect<sup>9</sup>. The implementation of filter circuit in CMOS technology with grounded components is highly desirable as it leads to miniaturization, low power consumption and integrated circuit realization. However, these advantages are at the expense of speed of operation,

which may be overcome by employing certain compensation techniques $^{6}$ .

In this paper, we present an all-pass/notch filter realized using low-voltage CCIIs. Though there exist several voltage mode all-pass/notch filter circuits given in literature<sup>8-19</sup>, but the circuit presented here enjoys the advantage of having high input impedance, equal valued grounded capacitors, independent control of filter function and filter gain. With two CCIIs, there exists no filter realization having high input impedance and grounded capacitors and thus still is a matter of research. There exists a similar circuit using three CCIIs but with unequal valued capacitors<sup>13</sup>. The proposed circuit can be directly replaced with translinear CCIIs where it uses much less passive components. The operation of these circuits has been verified by using PSpice in 0.5 µm technology at supply voltage of  $\pm 0.75$  V.

#### **2** Circuit Description

The working principle of CCII is characterized by the following relations:

 $I_Y = 0$ ,  $V_X = V_Y$  and  $I_Z = \pm I_X$  (+ sign for CCII+ and - sign for CCII-). Using these relations, the routine analysis of the circuit for all-pass/notch filter is shown in Fig. 1 which yields the following transfer function:

<sup>&</sup>lt;sup>1</sup>E-mail: susheelksharma@gmail.com

$$\frac{V_o(s)}{V_{in}(s)} = \frac{R_5}{R_3} \left[ \frac{s^2 C_1 C_2 R_1 R_2 + s(C_1 R_1 + C_2 R_2 - K C_1 R_2) + 1}{s^2 C_1 C_2 R_1 R_2 + s(C_1 R_1 + C_2 R_2) + 1} \right] \dots (1)$$

where  $K = \frac{R_3}{R_4}$  and for K = 2,  $R_1 = R_2 = R$  &  $C_1 = C_2 =$ 

C, Eq. (1) realizes a notch filter whose transfer function is given by

$$\frac{V_o(s)}{V_{in}(s)} = \frac{R_5}{R_3} \left[ \frac{s^2 C^2 R^2 + 1}{s^2 C^2 R^2 + 2s CR + 1} \right] \qquad \dots (2)$$

which gives  $\omega_0 = \frac{1}{CR}$  and Q = 0.5

Now if we choose K = 4,  $R_1 = R_2 = R$  and  $C_1 = C_2 = C$ , Eq. (1) realizes an all-pass filter whose transfer function is given by:

$$\frac{V_o(s)}{V_{in}(s)} = \frac{R_5}{R_3} \left[ \frac{s^2 C^2 R^2 - 2sCR + 1}{s^2 C^2 R^2 + 2sCR + 1} \right] \qquad \dots (3)$$

The phase angle ( $\phi$ ) is given by:

$$\varphi(\omega) = -2 \tan^{-1} \left( \frac{2\omega CR}{1 - (\omega CR)^2} \right) \qquad \dots \qquad (4)$$

It is observed that filter gain is controlled by  $R_5$  and filter function (*K*) is controlled independently by  $R_4$ . *K* can be controlled by  $R_3$  but that changes gain also. The circuit has high input impedance as input is applied to Y terminal of CCII and employs equal valued grounded capacitors.

### **3** Simulation Results

CCII+ used for realizing circuit in Fig. (1) is taken from Ref. 3, which is modified by using FGMOS current mirrors<sup>5, 6</sup>, as shown in Fig. (2). It has been simulated using PSpice for 0.5  $\mu$ m technology with supply voltage of ± 0.75 V. The W/L ratios for various transistors have been chosen as 25  $\mu$ m/0.5  $\mu$ m for M1 and M2, 4  $\mu$ m/0.5  $\mu$ m for M4, M6 and M7, 45  $\mu$ m/1  $\mu$ m for M8 and M10, 66  $\mu$ m/1  $\mu$ m for M3 and



Fig. 1-All-pass/notch filter



Fig. 2-CCII+ structure

M9 and 12 µm/0.5 µm for M5. The bias current ( $I_{bias}$ ) chosen is 100 µA. Simulation results show that it offers an input resistance of 2.53  $\Omega$  at port X, 10<sup>20</sup>  $\Omega$  at port Y and output resistance of 119.8 M $\Omega$  at port Z. The power consumed by the circuit is 1.62 mW. The current and voltage transfer ratios are almost unity with an error less than ± 0.2 %. The bandwidth for both current and voltage transfers has been found to be 100 MHz. CCII- is realized by inverting the output current of CCII+ using a bipolar FGMOS current mirror<sup>5</sup>. It offers output resistance of 243 M $\Omega$  at port Z and consumes 2.17 mW power. The bandwidth for current transfer is 16 MHz while for voltage transfer is 100 MHz.

The filter circuit is simulated for notch frequency of 318 kHz by choosing  $C_1 = C_2 = 500$  pF and  $R_1 = R_2 = 1$  k $\Omega$  and for different gains by choosing  $R_3 = 1$ k $\Omega$ ,  $R_4 = 0.5$  k $\Omega$  and  $R_5 = 1$  and 10 k $\Omega$  respectively. The simulated magnitude and phase responses are compared with the corresponding theoretical curves as shown in Figs 3 a and b respectively. The deviation in simulated curves from theoretical curves is found towards higher frequency, which may be attributed due to non-idealities of CCIIs. However, when the filter is simulated for lower critical frequency



Fig. 3(a)-Magnitude response of notch filter







Fig. 4(a)-Magnitude response of all-pass filter

( $f_0 = 3.18$  kHz), the simulated and theoretical curves are found to be identical and overlapping. The circuit offers input resistance of  $10^{20} \Omega$  and consumes 5.42 mW power. For simulating all-pass response, we have chosen  $R_3 = 2 \ k\Omega$ ,  $R_4 = 0.5 \ k\Omega$  and  $R_5 = 2$  and 20 k $\Omega$  respectively for different pass band gains. The comparative magnitude and phase responses are shown in Figs 4 (a and b) respectively.



Fig. 4(b)—Phase response of all-pass filter

#### **4** Conclusion

We have presented a low-voltage CCII based dual function filter that can realize both notch and all-pass filter responses. The filter function and gain are independently controllable by resistors. The circuit employs equal valued grounded capacitors and thus makes it suitable for chip implementation. Theoretical predictions have been supported by PSpice simulations carried out with a supply voltage of  $\pm 0.75$  V.

## Acknowledgement

Susheel Sharma thanks Prof S K Khosa, Former Head, Department of Physics and Electronics, University of Jammu, Jammu, for his encouragement, support and keen interest in this work. He also thanks University Grants Commission, New Delhi, Govt of India for awarding Teacher Fellowship under FIP scheme during tenth plan period.

#### References

- 1 Yan S & Sanchez-Sinencio E, *IEICE Trans. Fundamentals*, E00-A (2000).
- 2 Rajput S S & Jamuar S S, *IEEE Circuits and Systems Magazine*, 2 (2002) 24.
- 3 Rajput S S, *Low voltage current mode analog circuit structures and their applications*, Ph.D. thesis, Indian Institute of Technology, Delhi, 2002.
- 4 Ramirez-Angulo J, Choi S C & Altamirano G G, *IEEE Trans Circuits Syst.-I*, 42 (1995) 971.
- 5 Sharma Susheel, Rajput S S, Magotra L K & Jamuar S S, FGMOS based wide range low voltage current mirror and its applications (APCCAS-2002/IEEE, Bali, Indonesia), 2002, p. 331.
- 6 Sharma Susheel, Rajput S S, Mangotra L K & Jamuar S S, Analog Integrated Circuits and Signal Processing, 46 (2006) 281.
- 7 Sedra A S & Smith K C, *IEEE Trans Circuits Theory*, CT-17 (1970) 132.

- 8 Pal K, Electron Lett, 16 (1980) 639.
- 9 Liu Shen-Iuan Tsao Hen-Wai, *IEEE Trans. Circuits Syst.-I*, 38 (1991).
- 10 Shah N A, Iqbal S Z & Parveen B, *Indian J Pure & Appl Phys*, 42 (2003) 854.
- 11 Metin B, Toker A, Terzioglu H & Cicekoglu O, *Frequenz*, 57 (2003) 241.
- 12 Pandey N & Paul S K, Int J Electron, 91 (2004) 485.
- 13 Pal K & Singh R, *Electron Lett*, 18 (1982) 47.

- 14 Soliman A M, Microelectronics J, 29 (1998) 133.
- 15 Soliman A M, Frequenz, 53 (1999) 84.
- 16 Higashimura M & Fukui Y, Int J Electron, 65 (1988) 823.
- 17 Pal K, Microelectronics J, 22 (1991) 53.
- 18 Jiun-Wei Horng, *Computers and Electrical Engineering* 31 (2005) 81.
- 19 Kumar P, Pal K & Gupta G K, *Indian J Pure & Appl Phys*, 44 (2006) 398.