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Light assisted irreversible resistive switching in ultra thin hafnium oxide

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An ultra thin film (~5 nm) high-k Hafnium oxide dielectric, grown on a doped p-Si(100) substrate by the atomic layer deposition technique has been investigated for resistive and capacitive switching with and without illumination of light. As grown samples illustrate small non-switching leakage current under high applied electric fields and probe frequencies and trap charge assisted counter-clockwise capacitance–voltage behavior. A unique resistance switching was observed under illumination of 15–60 mW light. In the first cycle, the light assisted switching provide a $10^4 : 1$ resistance ratio, which diminishes in the next cycle onward, which may be due to irreversible charge injection in the oxide layers. The band offset and band match-up energy diagram for the charge carriers responsible for resistive switching and charge trapping near the interface have been demonstrated under the application of a bias electric field and light.

Introduction

Nowadays resistive random access memory (RRAM) has been considered the most promising non-volatile random-access-memory (NVRAM) for a variety of logic applications. A large number of potential binary and ternary oxides have been showing high speed resistance switching states and large ON/OFF resistance ratio useful for RRAM applications.^{1–3} These systems have profound potential for next generation logic and memory elements due to their low power consumption, excellent charge retention and easy to integrate with silicon.⁴ The simple structure for realization of RRAM device is a cross-bar structure with insulating oxide layer sandwiched between top and bottom metal electrodes. On the other hand, the basic criterion for complementary-metal-oxide-semiconductor CMOS logic devices is the direct integration of binary and ternary oxides with the silicon. These transition metals based binary and ternary oxides in their crystalline and amorphous phases have been considered in metal–insulator–semiconductor (MIS) configuration for next generation logic devices and metal–insulator–metal (MIM) configuration for the nonvolatile resistive switching elements.⁵ It is also very important to understand the photoconductivity of oxides integrated with silicon, which under illumination of light injects charge carriers across the interfaces and change the band match-up diagram structure.^{6,7} Ultra thin films and device structures of these materials were integrated with Si utilizing sophisticated equipments such as molecular-beam or electron beam deposition, pulsed laser

deposition, metal–organic chemical vapor deposition and atomic layer deposition techniques. Above mentioned techniques were widely used for fabrication of ultra thin films of HfO_2 ,^{8–11} TiO_2 ,¹² Al_2O_3 ,¹³ LaGdO_3 ,¹⁴ DyScO_3 ,¹⁵ SrTiO_3 (ref. 16) YCrO_3 (ref. 17) *etc.* which have been showing a tremendous potential for memory and logic applications.

Ultra thin hafnium oxide (HfO_2 : HFO) thin film is one of the most promising material among the high-k dielectrics which has been considered for resistive switching elements due to their high dielectric constant (~21), low leakage current, high optical band gap (~5.8 eV), and compatible with silicon.^{18,19} To utilize very low power consumption and multiple-memory logic states during the read and write process, a novel optical method has been demonstrated in resistive memory devices. Light assisted resistive logic states have been reported for Al_2O_3 oxide sandwiched between Pd and SiO_2/Si with controlled exposure to the top surface of alumina.²⁰ Other binary and ternary oxides have also shown an extra degree of freedom in resistive states under controlled illumination of light, which may be a significant development in the field of information and NVRAM technology.^{21–23} On the other hand, devices directly integrated on Si is highly sensitive to the illumination of moderate light intensity which partially or permanently changes the band offset alignment and creates photon assisted trap levels near the different interface. To understand the basic physics, band alignment behavior, reproducibility, and device life time, it is due to have methodical investigation on the functional properties of HfO_2 – SiO_2/Si heterostructures under different light ambient condition.

In this report, illumination of light on high-k HFO protective layer with semi transparent top gold metal electrode for Au/HFO/ SiO_2/Si heterostructure has been studied. Photon assisted charge transport from metal through the insulator layer is

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facilitated because of the minimal conduction band offset. The illumination of light with certain threshold electric (E)-field on heterostructure has permanently changed the high resistive states of device and the band alignment.

Experimental details

The ultra thin films of HfO_2 (4–5 nm) were fabricated using atomic layer deposition technique on SiO_2 (1 nm)/p-Si substrate. The details of the fabrication and deposition conditions are given elsewhere.^{12,24} As deposited amorphous phase of these films were changed to polycrystalline in nature after post annealing at 600 °C in nitrogen ambient. A high resolution transmission electron microscopy (TEM) image of $\text{HfO}_2/\text{SiO}_2/\text{Si}$ interface was obtained to check the inter-diffusion across the layers and crystalline nature of the high-k HFO. The crystal structure of the films was characterized using an X-ray diffractometer (PANalytical; Model; X'Pert³ MRD) employing grazing incidence and Cu-K α radiation. A Precision Multiferroic tester (Radiant Technologies Inc.), Keithley 236 source meter, and a halogen-tungsten light source with power (10–60 mW) were employed to evaluate the effect of light on current–voltage and capacitance–voltage measurements. The spectral response of the light source was similar to the standard halogen-tungsten lamp having filament temperature near 3200 K to 2800 K. The intensity of the light was modified using an in-house fabricated set up in which the lens was attached with the halogen-tungsten lamp. The power of light source was decided by various distances between source lamp and lens which finally fall on the devices with different power. The in-house light source setup for various lengths was calibrated with the standard photodetector with various head assembly to measure the accurate light power with error (± 2 mW). The standard photodetector was manufactured by United Detector Technologies; model QED-200 quantum efficiency detector, and AUV head assembly (model: 222 & 261). Semi transparent gold electrode (~ 40 nm) was deposited using shadow mask of area 0.0004 cm² by thermal evaporation technique to fabricate the MIS structure for electrical measurements. The optical transparency of Au electrode is around 20% compared to the transparent conducting oxide (indium tin oxide) film on glass. Current–voltage (I – V) and capacitance–voltage (C – V) data were obtained with and without continuous illumination of visible light.

Results and discussion

Schematic diagram of Au/HFO/SiO₂/Si heterostructure is shown in Fig. 1(a). Visible light was illuminated over the semi transparent top Au electrode. Fig. 1(b) shows the morphology of the polycrystalline HFO dielectric with thickness 4–5 nm. The local structure of the ALD grown HFO mainly consists the mixture of monoclinic/orthorhombic phase depending on the annealing ambient.^{12,23} A thin layer of SiO₂ (~ 1 nm) was formed at the interface of the HfO₂ and Si during post-annealing process. In the past, detailed studies on the transport properties have been carried out over small gate area 300 × 300 nm² using atomic force microscopy/scanning tunneling microscopy tip and found

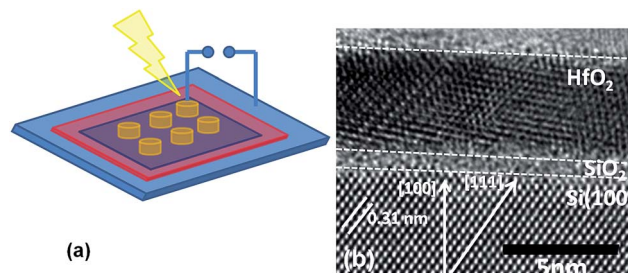


Fig. 1 (a) show schematic diagram of Au/HFO/SiO₂/Si heterostructure, (b) HRTEM image of 600 °C annealed heterostructure with bar scale of 5 nm.

interesting role of grain boundaries in the kinetics and charge separation under application of E-field responsible for device failure. In present study, we used the large gate area 0.0004 cm² and direct current measurement technique (micro manipulators) for I – V and C – V measurements. Grazing incidence X-ray diffraction (GIXRD) was performed to understand the global microstructure and crystalline quality of 4–5 nm HfO₂ thin films. It indicates that films were polycrystalline in nature having monoclinic crystal structure. Note that GIXRD was carried out for 5 nm thin films and it is obvious to have poor signal to noise ratio in GIXRD data To enhance GIXRD signal to noise ratio and clear display of GIXRD peaks, raw data were smoothen for $\pm 2\%$ and demonstrated for the present study. GIXRD peaks were successfully indexed for monoclinic crystal structure as shown in Fig. 2 and well matched with the 2 nm to 20 nm MOCVD grown crystalline HfO₂ thin films by A. Milanov *et al.*²⁵ and Arne Baunemann *et al.*²⁶

To further check the capacitive performance of MIS capacitors, a typical C – V response of heterostructure was investigated in the frequency range from 1 kHz to 100 kHz at room temperature under dark condition (Fig. 3(a) and (b)). Well defined counterclock wise C – V responses were obtained at various probe frequencies which clearly shows accumulation at negative gate bias voltages and depletion at positive gate bias voltages. Ideally, the high-k dielectric gate should not show any hysteresis in the CV response but there is always trap charges at

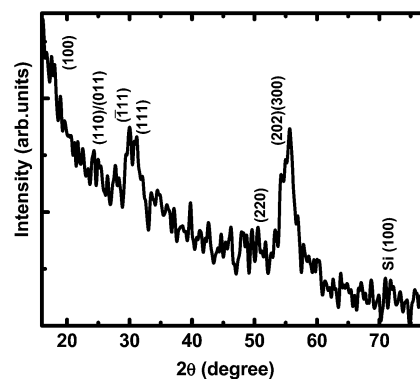


Fig. 2 Room temperature grazing incidence X-ray diffraction patterns of Au/HFO/SiO₂/Si heterostructure.

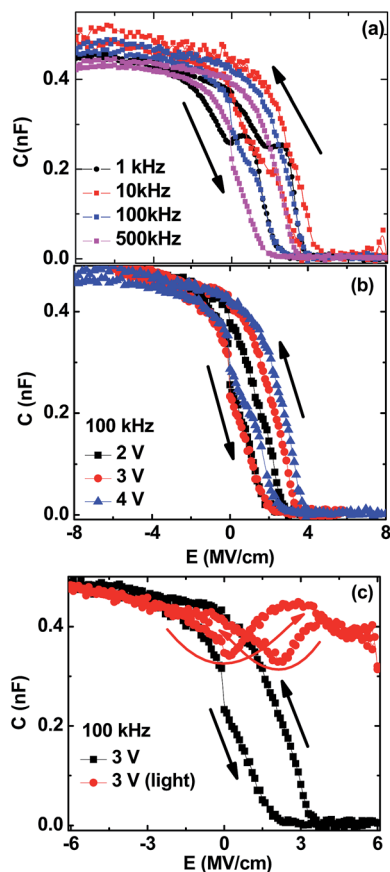


Fig. 3 Capacitance–Electric field (C – E) hysteresis of Au/HFO/SiO₂/Si heterostructure, (a) as function of frequency (1–100 kHz), (b) as function of applied E -field at 100 kHz, and (c) at 100 kHz and $6 \text{ MV cm}^{-1} \text{ E}^{-1}$ -stress with and without illumination of 60 mW light.

the interface which develops the hysteresis in C – V curves.²⁷ The observed C – V hysteresis behavior of MIS structure exhibited 1–2 V memory windows in the range of 1–100 kHz, depending on probe frequencies and E -field. The up and down sweeping of C – V curves for 1 kHz probe frequency show a kink near the depletion regions *i.e.* boundary of accumulation and depletion region suggests high contribution of electronic space charge carriers for low probe frequencies. Each C – V curves show a considerable voltage-axis shift towards positive side due to the presence of interface states. The flat-band voltage shifted toward negative bias as the probe frequency was increased. It is clear from the Fig. 3(b) that the memory window of the C – V hysteresis increases with increase in E -field; however it significantly reduces with increase in probe frequencies. Memory window should provide the different logic states for writing and reading the data bits.^{28,29} Fig. 3(c) shows the C – V of MIS structure with and without light illumination at 100 kHz and reasonable low E -field stress ($\sim 6 \text{ MV cm}^{-1}$ to avoid breakdown). Interestingly, presence of light populates the charge carriers at p-Si gate and stops the device to reach the inversion states. The depletion region displays two minima like the inverted butterfly loops. These developments are mainly due to the charge carrier injections into the HfO₂ ultra thin films. The counter-clockwise

C – V hysteresis ruled out the possible polar nature of the HfO₂ and trap assisted memory window in C – V curves at high probe frequencies. These are due to trapped charges at the interfaces or injected charges in high- k dielectrics under application of E -stress and illumination of light.

Fig. 4(a) and (b) show the current–voltage (I – V) characteristic of the Au/HFO/SiO₂/p-Si heterostructure in dark and under illumination of moderate light energy. Several devices were tested for resistive switching in dark, none of them switched under high E -field ($\sim 8 \text{ MV cm}^{-1}$), and gave extremely low leakage current suitable for next generation logic elements in contrast to earlier report.³⁰ These devices were later illuminated by moderate visible light with power 60 mW which in turn switched the MIS current from high to low resistance states. The average switching E -field and high to low resistance ratio lies in the range of ~ 2.8 – 3.3 MV cm^{-1} and 10^4 :1, respectively depending on quality of device. These small variations in switching fields may be due to inhomogeneous distribution of grain boundaries in large device area.^{12,31} Please note that we have not mentioned the energy density of light source in present investigation, because during illumination of light on devices, large portion of silicon wafer which hold the devices also received light and contribute in transport properties. Interestingly it has been found that once the device switched under light, it never recover the original high resistance, charge

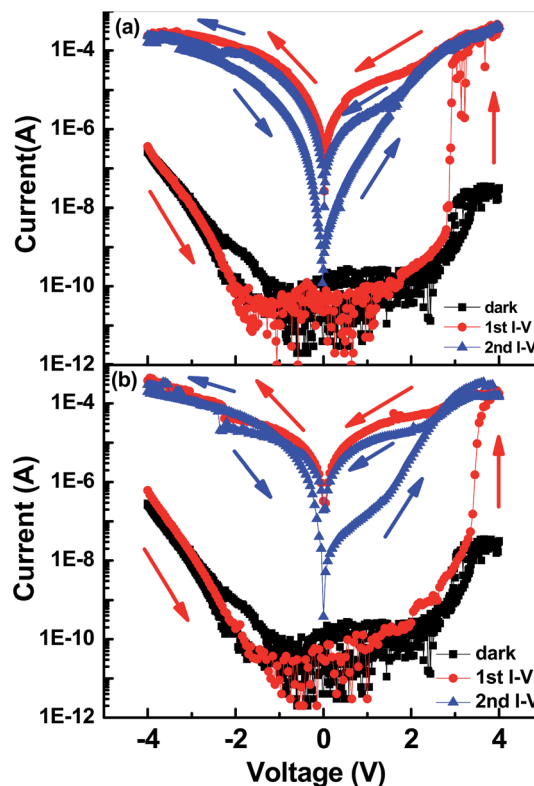


Fig. 4 Current–voltage (I – V) full cycle curves of Au/HFO/SiO₂/Si heterostructure, (a) device 1, and (b) device 2. Similar I – V curves were observed for both the devices in dark. Giant Irreversible I – V switching was observed on as grown sample and represented by 1st I – V run under illumination of light. 2nd I – V run indicates the current characteristic of device after first giant irreversible switching.

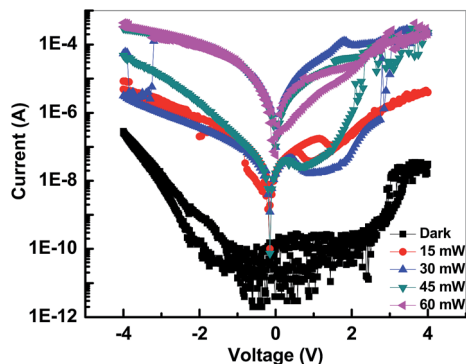


Fig. 5 Illustrates the current–voltage (I – V) curves of Au/HfO₂/SiO₂/Si heterostructure under dark and after illumination of light from 15 to 60 mW.

injection may permanently changed the band off set and create new impurities charge/trap levels as shown in the band diagram and breakdown mechanism of devices under light (Fig. 6 and 7). These devices were further checked for I – V behavior under illumination of light which display nonlinear I – V curve with high current level and marginal switching on either side of the MIS device. It clearly shows that illumination of light permanently damage the high resistance state of MIS device, the current mechanism can be explained using Poole–Frenkel (PF) or Schottky emission (SE) process.³²

A further I – V investigation on the as grown sample with various light illuminations was conducted to check the critical light intensity responsible for permanent damage of high resistance state (Fig. 5). Even small amount of light creates trap levels in the heterostructure and shift the high resistance state towards low resistance state. Utilization of 15 mW light intensity lowered at least one order of resistance without any switching, with further increase in light intensity, MIS structure demonstrates switching but starts from the initial resistance state developed due to illumination of 15 mW intensity. The light intensity was increased from 15 mW to 60 mW to check the switching behavior. The light intensity nearly 30 mW switched the device from high to low resistance state which further re-set to high resistance state during the negative bias E-field which provides a suitable condition for the nonvolatile resistive memory. However the behavior and magnitude of resistive switching varies from device to device and not robust and reproducible in many cases which may be due to the presence and distribution of grain boundaries in that particular device.²⁸ The light intensity ~ 45 mW may considered as critical intensity for unrecoverable low resistance state of device and excess charge injection which creates permanent trap levels on either side of the device. It is also clear that with slow and step wise increase in light intensity provide a condition that one cannot observe sharp switching. It suggests that light illumination slowly creates the trap levels in devices which never recovered after removal of light. These devices illustrate nonlinear current response with moderate memory window during forward and reverse (\pm) E-field switching even after development of permanent trap levels and charge carriers.

Fig. 6 demonstrates the energy level diagram of Au/HfO₂/SiO₂/p-Si hetero-structure. Here Φ is the Au work function 5.1 eV; χ is the semiconductor electron affinity (1.8 eV for HfO₂; 0.9 eV for SiO₂; and 4.05 eV for Si); E_g is the bandgaps (5.8 eV for HfO₂; 8 eV for SiO₂; and 1.1 eV for Si); E_v and E_c are the valence and conduction band edges.^{2,3} In real scenario, the vacuum level can be obtained with slight different position for each material due to charge injection. Two trap levels have been marked in the regions of HfO₂ and SiO₂ due to charge injections or accumulation after illumination of light. These trap levels are the origin of reduction of barrier height which easily inject electrons and holes in either side of heterostructure under application of external E-field and presence of light. The Schottky barrier for charge injection is relatively higher from Si into SiO₂/HfO₂ interface; on the other hand trapped charge carriers reduce the electron barrier height near the conduction band. The band match-up demonstrates that the existing MIS structures have a very high band off-set value but it significantly reduces due to development of impurities, trapped charges, and depletion region under illumination of light.

Fig. 7(a) and (b) show the possible change in the barrier heights and the development of charge carriers at interfaces under illumination of white light and the application of positive and negative bias E-field, respectively. Under illumination of light, electrons accumulated the Si–HfO interface and developed the depletion (DL) region (Fig. 7(c)) which creates high resistance states in the device. The devices switched abruptly from high to low resistance state under application of critical applied forward electric field which may be due to the abrupt breakdown the DL regions which set the device at low resistance state. The breakdown of DL region provides the condition to charge carriers for fast and abrupt flow in the external electric circuit and set the device for permanent low resistance state which never recovers under application of negative gate voltage. We elucidate the abrupt change in the current as a modulation of trapped charges across the HfO/Si interface.

To summarize, MIS structure with HfO as high-k dielectric was investigated for capacitive and resistive switching with and without illumination of light. A counter clockwise C – V with

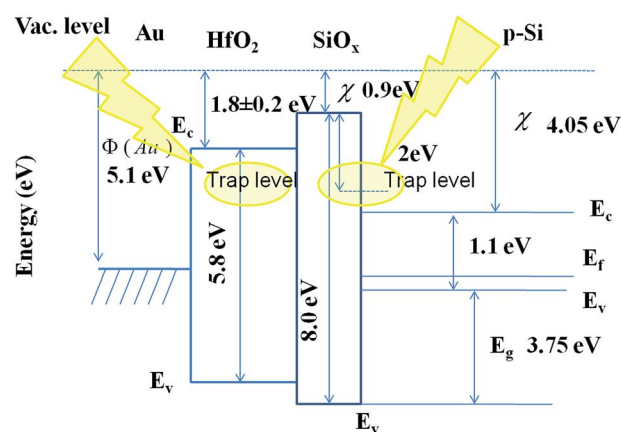


Fig. 6 Summary of band alignment and interface of Au/HfO₂/SiO_x/p-Si ($x = 2$).

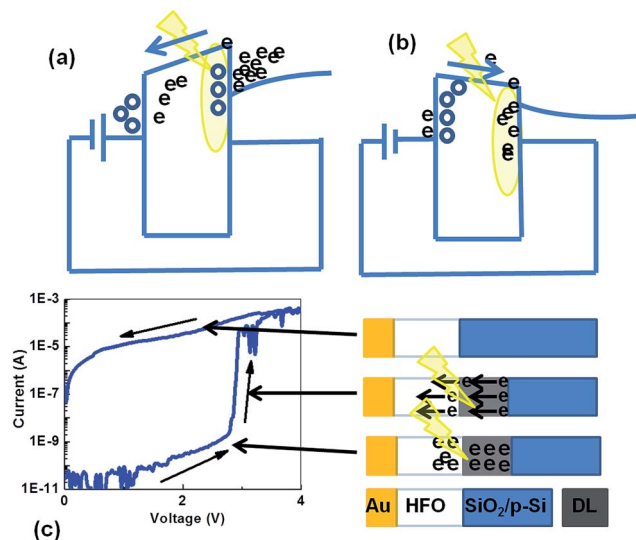


Fig. 7 Band alignment and interface condition of Au/HfO₂/SiO_x/p-Si ($x = 2$) heterostructure, (a) under positive gate voltage and illumination of white light, (b) under negative gate voltage and illumination of white light, (c) switching mechanism of high, switched, and low resistance states with possible development of depletion region and its breakdown condition.

1–2 V memory windows was obtained for MIS structure for high (1–100 kHz) probe frequency in dark that suggests the trap charge assisted capacitive memory developed in the device during the sweeping of gate voltage from negative to positive bias and then again back to negative voltage. Illumination of light has modified the inversion center of the heterostructure and provides an inverted butterfly loop in $C-V$ spectra. Reversible resistive switching was observed below critical light intensity and E-field due to transient trap charges in devices, however the observed phenomena was not robust due to the uneven distribution of grain boundaries in the matrix. A sharp but irreversible resistive switching with $10^4 : 1$ resistance ratio was observed under illumination of light. It is mainly due to charge injection and permanent creation of trap levels in oxides. A small amount of light may change HFO gated MIS structure from not switchable to switchable resistive states with permanent shift of their high resistance states to several order of low resistance states. This report provides an insight to the researchers and scientists working in area of high- k dielectrics directly integrated with silicon for possible application for resistive switching under moderate and low power light illumination and possible device failure under excess dosage of light illumination.

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